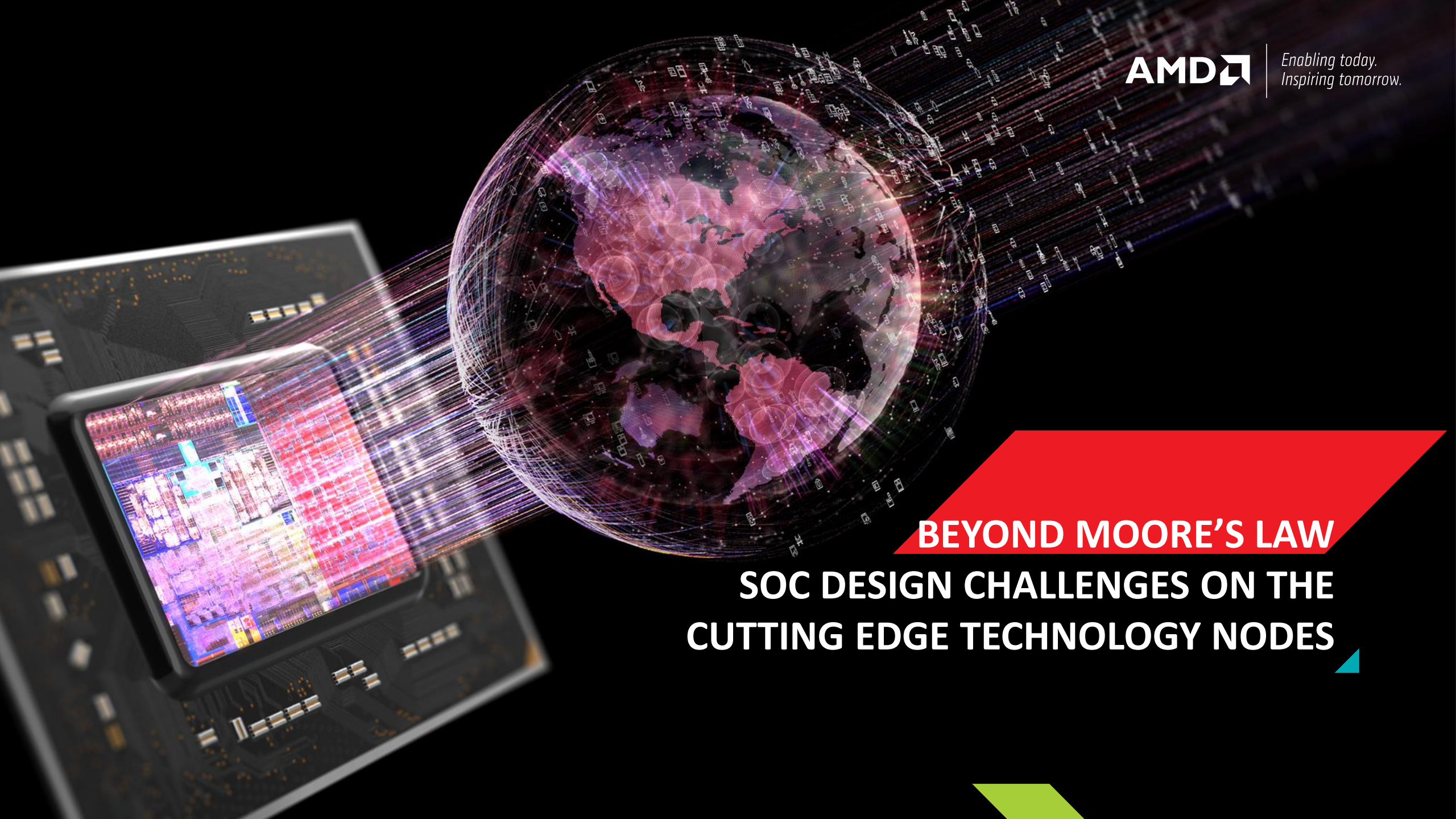


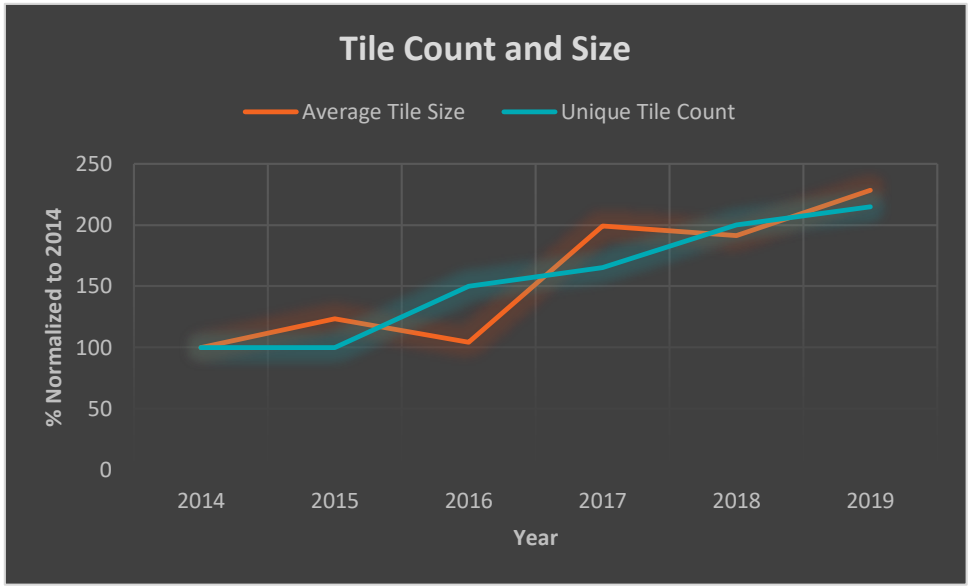
AMD
Enabling today.
Inspiring tomorrow.

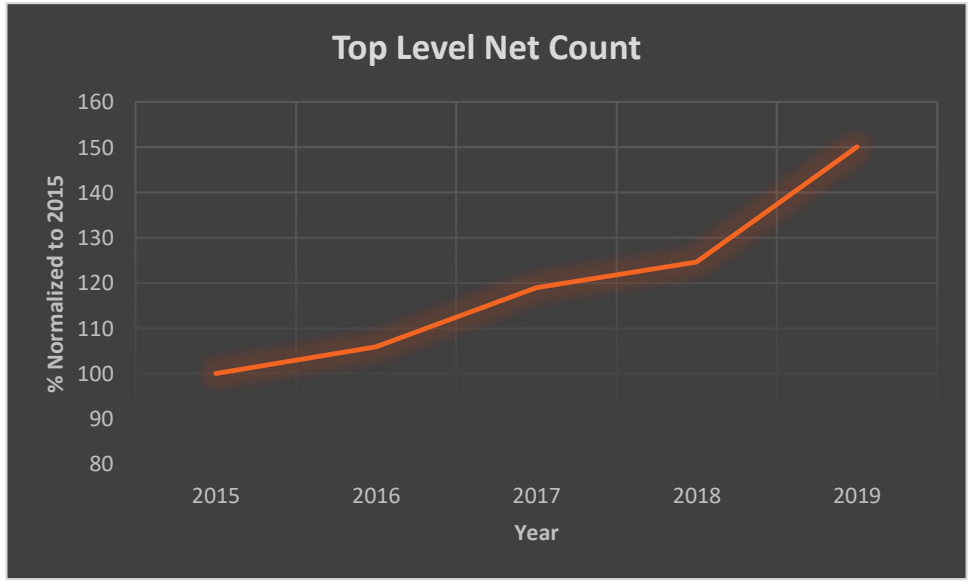
BEYOND MOORE'S LAW

SOC DESIGN CHALLENGES ON THE CUTTING EDGE TECHNOLOGY NODES

DESIGN : INCREASING SIZE

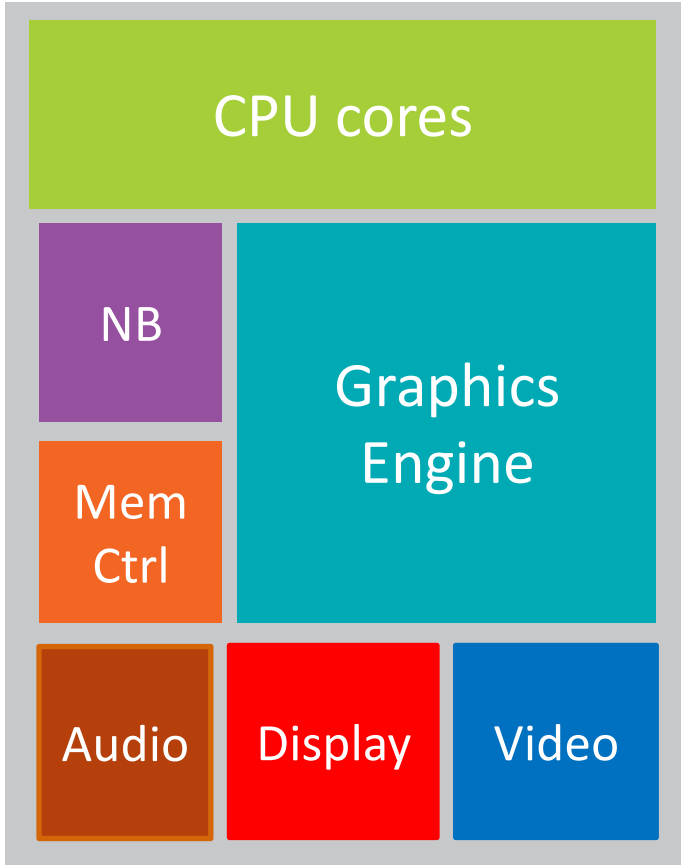
- Tile Count is increasing steadily
  - ~2x increase in unique tile count over 5 years
- Instances Per Tile is increasing steadily
  - ~2x increase in average instance count over 5 years
  - Flow runtime and capacity improvements needed to continue this trend
- Top level net count also increasing
  - Floor-planning and construction challenge
  - Flop stage insertion creates a dependency between floorplan and RTL
  - Top level timing closure is the critical path to tape-out
  - Wire dominated critical paths can limit frequency scaling at higher voltages





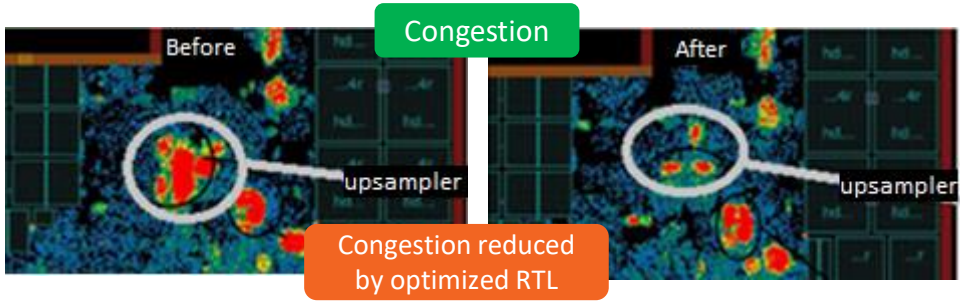
DESIGN : INCREASING COMPLEXITY

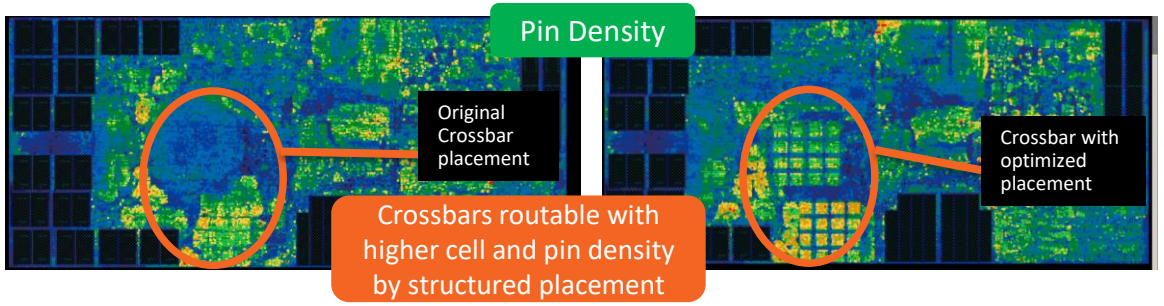
- AMD SOC's can have many IP's integrated
  - Including CPU cores, Graphics Engine, Video Encoder/Decoder, Display Engine, Audio, memory controller, northbridge
- Each IP can have different design requirements
  - From a few tiles to >100 tiles for a single IP
  - Clock frequencies from 100Mhz to multi-GHz
  - Multiple clock distribution techniques can be used depending on skew, insertion, and power requirements
  - Multiple DFP techniques can be used, from basic clock gating and multi-Vt to cutting edge techniques
  - Data busses can add repeater stages depending on floorplan and frequency requirements
  - Optimized synthesis and P&R recipe for each tile to hit PPA targets
- SOC-level integration requirements
  - Flexible and expandable "fabric" needed to interconnect IP at SOC level
  - Complex floorplan constraints to meet LUP, ESD, latency, and package requirements



DESIGN : STRONG LINK BETWEEN LOGICAL AND PHYSICAL DESIGN

- In the past there has been a wall between logical and physical design
  - Both would work independently to meet their design goals
  - Synthesis netlist "thrown over the wall" to PD for layout and GDS generation
- 2-way feedback is now critical to meet aggressive design requirements
- Logic designers work to reduce Levels-of-Logic and routing congestion in their design based on physical design feedback
- Physical design team can implement custom layout solutions optimized for certain logical structures
  - Examples include Flop or latch array and signal crossbars



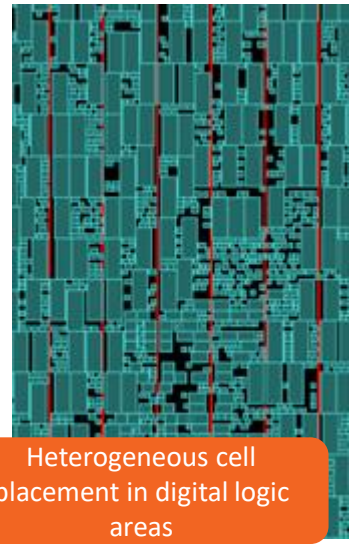


Timing Fix Technique	Original RTL	Optimized RTL
Rewrite RTL code for "median" function and restructure large MUX	**54 Levels of Logic, in synthesis**	**31 Levels of Logic, in synthesis**

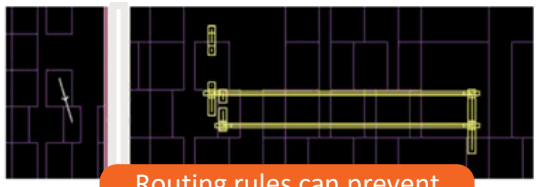
42% reduction in Levels of Logic with optimized RTL

TECHNOLOGY : NEW NODES BRING NEW CHALLENGES

- Designing in cutting edge technology nodes has new challenges for Physical Design engineering teams, flows, and tools
  - Growth in design database sizes and DRC rule count
    - and associated storage and compute requirements
  - Cell and Macro placement challenges
    - Heterogeneous placement in digital logic areas with more cells being multi-row height
    - Cell placement more likely to be disturbed by power routing
  - Wiring challenges
    - Uni-directional routing layers, especially on lower layers used for pin access
    - Multi-patterning and associated colour restrictions
    - Resistance and Capacitance can change significantly between layers in the metal stack
    - Number of tracks can change significantly between layer types
  - Quantized transistor size scaling with FinFET



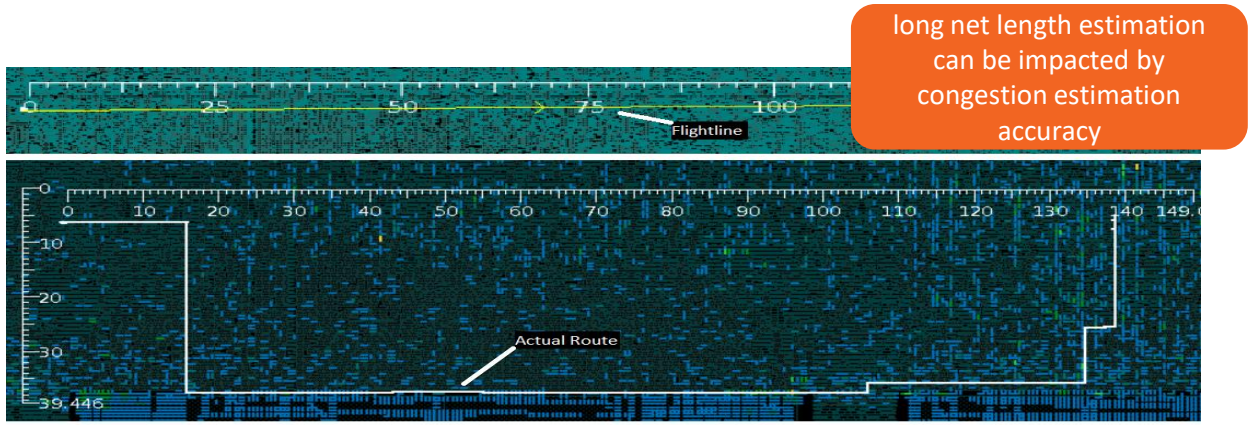
Heterogeneous cell placement in digital logic areas

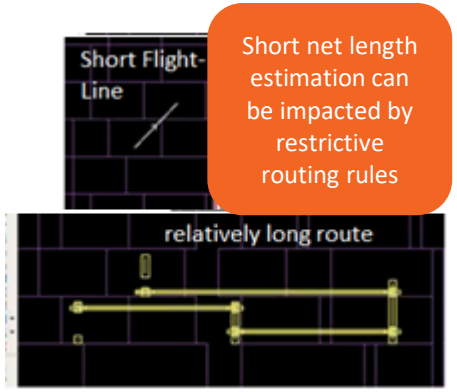


Routing rules can prevent easy connections using same layer jogs

FLOWS AND TOOLS : PRE-ROUTE TO POST-ROUTE TIMING CORRELATION

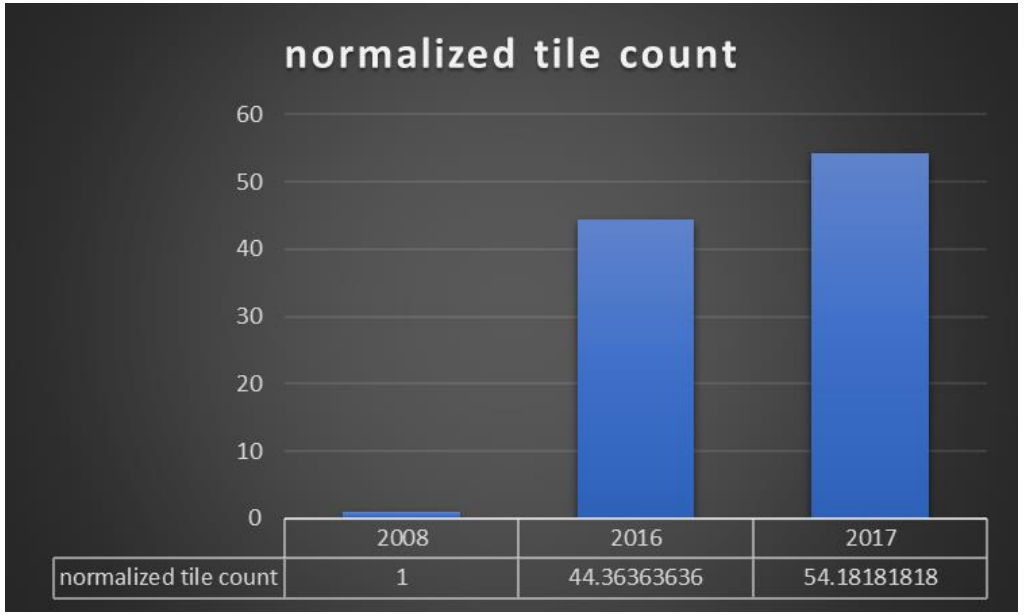
- Strong correlation between pre-route and post-route timing is important for design convergence
- R and C estimation can be off due to inaccuracy in route length and layer assignment
  - Post-route wire length almost always significantly longer than pre-route length estimation
  - Post-route metal assignment varies greatly based on route length, especially for shorter lengths
    - A route length estimation error here can lead to a large RC estimation error

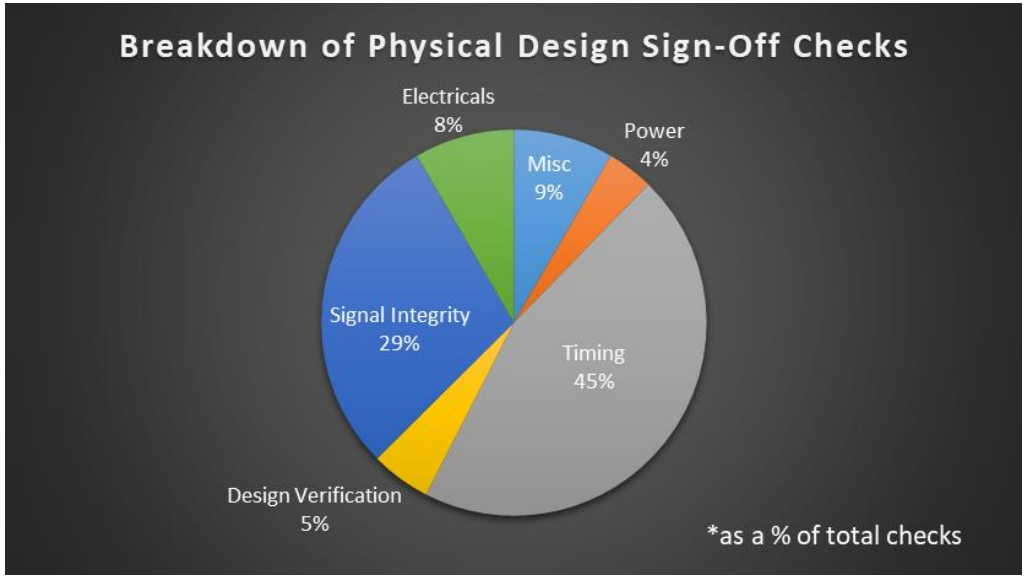




EXECUTION : PHYSICAL DESIGN EVOLUTION AND EXECUTION CHALLENGES

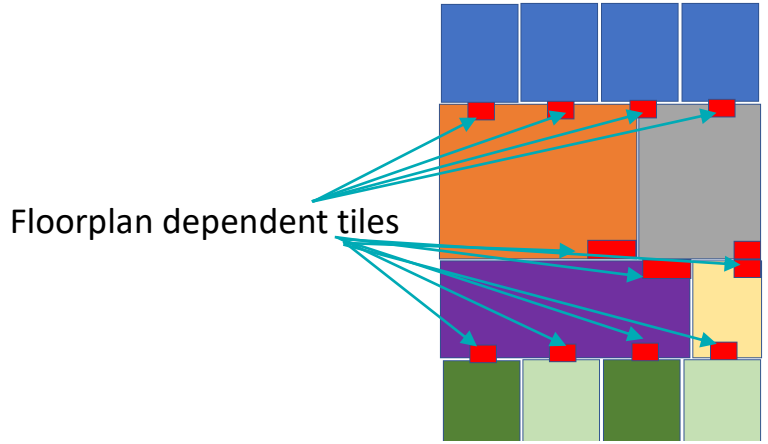
- Exponential growth
- Massive complicated design
  - > 100 physical design metrics are tracked
  - > 1000 logs / reports generated in P&R flows
- Large global team size, tight schedule
- Divide and conquer
- Detailed milestones / checklists per function along the project execution schedule
- Clear and solid plans needed up-front

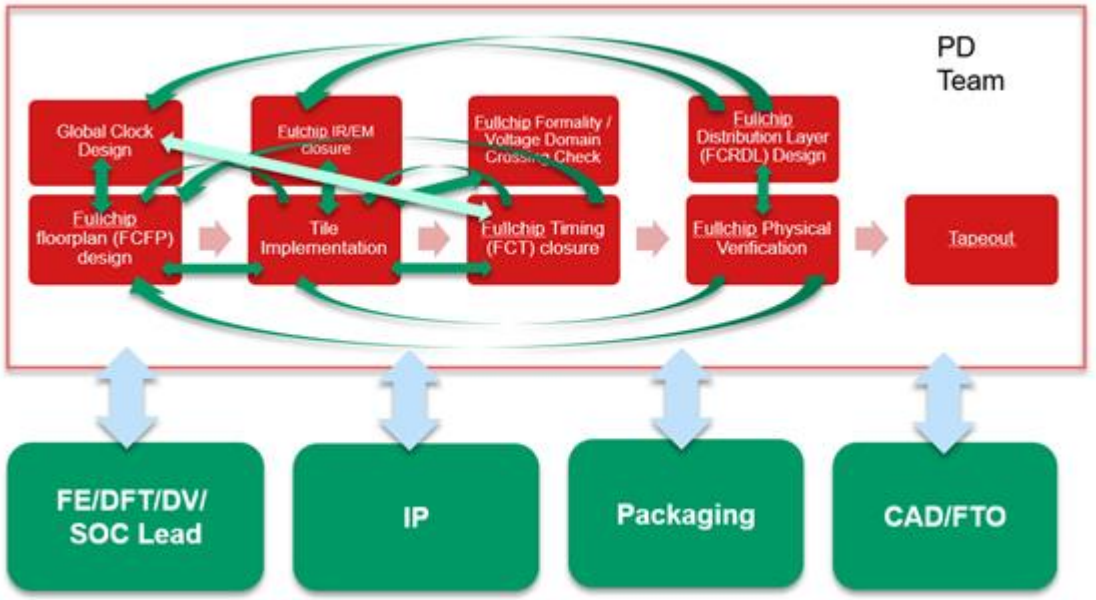




EXECUTION : PHYSICAL DESIGN EVOLUTION AND EXECUTION CHALLENGES

- Physical design implementation has increased influence on the RTL design development and the PPA (power performance area)
- Design architecture and topology is dependent on physical floorplan
- Achievable PPA needs to be verified with physical design implementation results
- Complicated feedback network between functions
- Timely feedback is needed to improve the RTL design





DISCLAIMER & ATTRIBUTION

The information presented in this document is for informational purposes only and may contain technical inaccuracies, omissions and typographical errors.

The information contained herein is subject to change and may be rendered inaccurate for many reasons, including but not limited to product and roadmap changes, component and motherboard version changes, new model and/or product releases, product differences between differing manufacturers, software changes, BIOS flashes, firmware upgrades, or the like. AMD assumes no obligation to update or otherwise correct or revise this information. However, AMD reserves the right to revise this information and to make changes from time to time to the content hereof without obligation of AMD to notify any person of such revisions or changes.

AMD MAKES NO REPRESENTATIONS OR WARRANTIES WITH RESPECT TO THE CONTENTS HEREOF AND ASSUMES NO RESPONSIBILITY FOR ANY INACCURACIES, ERRORS OR OMISSIONS THAT MAY APPEAR IN THIS INFORMATION.

AMD SPECIFICALLY DISCLAIMS ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. IN NO EVENT WILL AMD BE LIABLE TO ANY PERSON FOR ANY DIRECT, INDIRECT, SPECIAL OR OTHER CONSEQUENTIAL DAMAGES ARISING FROM THE USE OF ANY INFORMATION CONTAINED HEREIN, EVEN IF AMD IS EXPRESSLY ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

ATTRIBUTION